IN THE CLAIMS

1. (original) A method of setting a logic state of a memory cell, comprising:
applying a first potential to a control gate of the memory cell, wherein the first potential has a first polarity;
applying a second potential to a first source/drain region and a second source/drain region of the memory cell, wherein the second potential has a second polarity;
applying the second potential to a first well containing the first and second source/drain regions; and
applying a third potential to a second well, wherein the second well is underlying the first well and is coupled to the first well through a PN junction.

2. (original) The method of claim 1, wherein the first potential is a positive voltage and the second potential is a negative voltage.

3. (original) The method of claim 2, wherein the first potential is within the range of approximately 5V to 15V and the second potential is within the range of approximately –5V to –15V.

4. (original) The method of claim 2, wherein the third potential is approximately 0V.

5. (original) The method of claim 4, further comprising:
applying a ground potential to a substrate underlying the second well.

6. (original) A method of setting a logic state of a memory cell, comprising:
applying a first potential to a control gate of the memory cell, wherein the first potential has a first polarity;
applying a second potential to a first source/drain region and a second source/drain region of the memory cell, wherein the second potential has a second polarity;

applying the second potential to a first well containing the first and second source/drain regions; and

applying a third potential to a second well underlying the first well, wherein the second well is coupled to the first well through a PN junction and wherein the third potential has the second polarity.

7. (original) The method of claim 6, wherein the first potential is a negative voltage and the second potential is a positive voltage.

8. (original) The method of claim 7, wherein the first potential is within the range of approximately –5V to –15V and the second potential is within the range of approximately 5V to 15V.

9. (original) The method of claim 7, wherein the third potential is within the range of approximately 5V to 15V.

10. (original) The method of claim 9, further comprising:
applying a ground potential to a substrate underlying the second well.

11. (original) A method of setting a logic state of a memory cell in an array of memory cells, comprising:

applying a first potential to a word line associated with the memory cell in a first column(s) of memory cells of a plurality of columns of memory cells, wherein the first potential has a first polarity;

applying a second potential to a first source/drain region and a second source/drain region of the memory cell, wherein the second potential has a second polarity;

applying the second potential to a first well of the first column, where the first well contains the first and second source/drain regions;

applying a third potential to a first well of each of the remaining columns of memory cells of the plurality of columns; and

applying a fourth potential to a second well, wherein the second well is underlying the first wells of the plurality of columns and is coupled to each of the first wells through a PN junction.

12. (original) The method of claim 11, wherein the first potential is a positive voltage and the second potential is a negative voltage.

13. (original) The method of claim 12, wherein the first potential is within the range of approximately 5V to 15V and the second potential is within the range of approximately –5V to –15V.

14. (original) The method of claim 12, wherein the fourth potential is approximately 0V.

15. (original) The method of claim 14, further comprising:
applying a ground potential to a substrate underlying the second well.

16. (original) The method of claim 12, wherein the third potential is approximately 0V.

17. (original) A method of setting a logic state of a memory cell in an array of memory cells, comprising:

applying a first potential to a word line associated with the memory cell, wherein the memory cell is in a first column and the first potential has a first polarity;

applying a second potential to a first source/drain region and a second source/drain region of the memory cell, wherein the second potential has a second polarity;

applying the second potential to a first well of the first column, wherein the first well contains the first and second source/drain regions;

applying a third potential to a first well of a second column; and

applying a fourth potential to a second well underlying the first wells of the first and second columns, wherein the second well is coupled to the first wells through a PN junction and wherein the fourth potential has the second polarity.

18. (original) The method of claim 17, wherein the first potential is a negative voltage and the second potential is a positive voltage.

19. (original) The method of claim 18, wherein the first potential is within the range of approximately –5V to –15V and the second potential is within the range of approximately 5V to 15V.

20. (original) The method of claim 18, wherein the fourth potential is within the range of approximately 5V to 15V.

21. (original) The method of claim 20, further comprising:
applying a ground potential to a substrate underlying the second well.

22. (original) The method of claim 18, wherein the third potential is approximately 0V.

23. (original) The method of claim 18, wherein the third potential is within the range of approximately 5V to 15V.

24. (original) A method of forming a column of non-volatile memory cells, comprising:
forming two isolation trenches in a substrate;

forming a first well between the isolation trenches, wherein the first well has a first conductivity type;

forming a first source/drain region and a second source/drain region in the first well, wherein the first source/drain region is laterally separated from the second source/drain region to define an intermediate channel region and wherein the first and second source/drain regions have a second conductivity type different than the first conductivity type;

forming a second well underlying and in contact with the isolation trenches, wherein the second well has the second conductivity type;

forming a tunnel dielectric overlying at least the channel region;

forming a floating gate overlying the tunnel dielectric;

forming a control gate overlying the floating gate; and

forming an interlayer dielectric between the floating gate and the control gate.

25. (original) The method of claim 24, wherein forming two isolation trenches in the substrate further comprises forming two trenches in the substrate and filling the trenches with a dielectric material.

26. (original) The method of claim 24, wherein forming the first wells further comprises conductively doping portions of the substrate.

27. (original) The method of claim 26, wherein conductively doping the substrate further comprises ion implantation of a first dopant species.

28. (original) The method of claim 24, wherein forming the first and second source/drain regions further comprises conductively doping portions of the first well to the second conductivity type using a second dopant species.

29. (original) The method of claim 28, wherein forming the second well further comprises performing a deep implant of a third dopant species.

30. (original) The method of claim 29, wherein the third dopant species is different than the second dopant species.

31. (original) A method of forming a non-volatile memory cell, comprising:
forming two isolation trenches in a substrate, wherein each isolation trench contains a dielectric material;
conductively doping an exposed surface of the substrate to a first conductivity type between the isolation trenches, thereby forming a first well between the isolation trenches;
conductively doping a first portion and a second portion of a surface of the first well to a second conductivity type opposite the first conductivity type, wherein the first portion of the first well is laterally separated from the second portion;
conductively doping a portion of the substrate underlying and in contact with the isolation trenches to the second conductivity type;
forming a first dielectric layer overlying a surface of the first well;
forming a first conductive layer overlying the first dielectric layer, wherein the first conductive layer is capable of holding a charge;
forming a second dielectric layer overlying the first conductive layer; and
forming a second conductive layer overlying the second dielectric layer.

32. (original) The method of claim 31, wherein each dielectric is selected from the group consisting of silicon oxides, silicon nitrides and silicon oxynitrides.

33. (original) The method of claim 31, wherein the first conductive layer comprises a conductively-doped polysilicon material.